



正基科技股份有限公司

SPECIFICATION

PRODUCT NAME : AP5281SR

REVISION : 0.7(WEB)

DATE : Aug. 28th , 2026

Customer APPROVED	
Company	
Representative Signature	

PREPARED	REVIEW			APPROVED	DCC ISSUE
	PM	QA	ET		

正基科技股份有限公司



AP5281SR Data Sheet

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Revision

Revision	Date	Description	Revised By
0.1	2025/10/22	-- Preliminary release	May
0.2	2025/12/23	-- Modify Pin Define	May
0.3	2026/01/31	-- Update RF Spec	Jason
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0.5	2026/04/02	--Added WIFI6E Product feature	Howard
0.6	2026/08/06	-- Update Pin out	Jason
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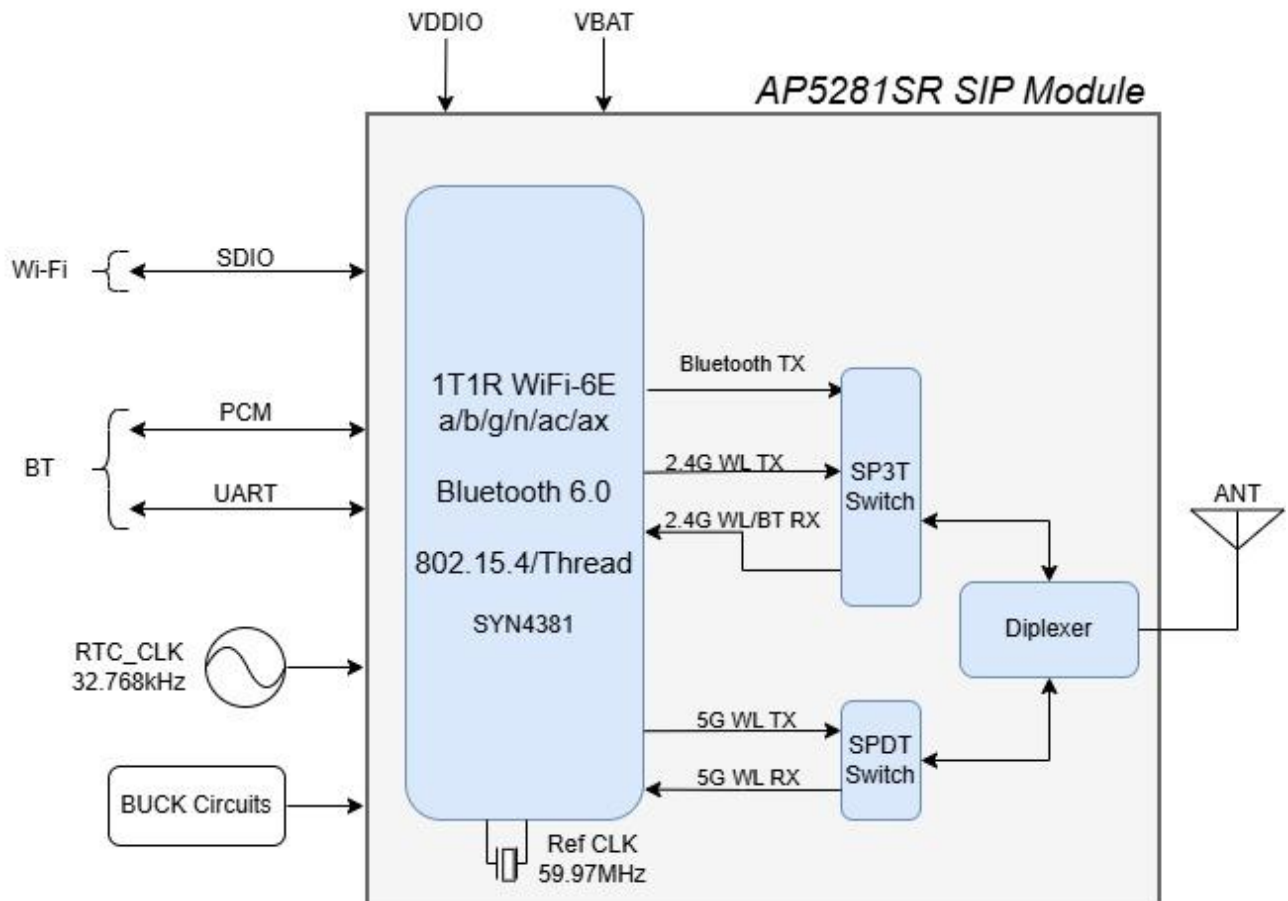
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1. Introduction

1.1 Overview

The AMPAK Technology® AP5281SR is a fully Wi-Fi 6E and Bluetooth and IEEE 802.15.4/Thread functionalities module with seamless roaming capabilities and advance security, also it can associate with different vendors' Wi-Fi 6E or legacy Access Points / Routers and run up to PHY rate of 600Mbps with single stream. Furthermore, AP5281SR included SDIO v3.0 interfaces by proper setting for Wi-Fi, UART/ PCM interface for Bluetooth, UART interface for IEEE 802.15.4/Thread. In addition, this compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for tablet, OTT box and portable & mobile devices.



1.2 Product Features

IEEE 802.11 Key Features

- 802.11ax/ac/a/b/g/n compliant
- Radio band support for 2.4 / 5 / 6 GHz band including 6GHz UNII-5,6,7,8
- Support 802.11ax & legacy for 2.4 / 5 GHz band
- Support 802.11ax only for 6GHz band
- Lead-free & Halogen-free design which is compliant with ROHS requirements.
- TX and RX low-density parity check (LDPC) support for improved range and power efficiency.
- Single-stream spatial multiplexing up to 600 Mbps data rate.
- 20, 40, 80 MHz bandwidth channels with optional SGI (1024 QAM modulation) for 5 / 6 GHz bands
- 20MHz channels for 2.4 GHz band with optional SGI (1024 QAM modulation)
- Supports standard SDIO v3.0/v2.0.
- Supported Partial RU(Resource Unit) in 802.11ax.
- Supported non-HT(802.11a) preamble in 6GHz.

Bluetooth Key Feature

- BT host digital interface:
 - HCI UART (up to 4 Mbps)
 - PCM for audio data
- Complies with Bluetooth Core Specification Version 6.0 with provisions for supporting future specifications. With Bluetooth Class 1 or Class2 transmitter operation.
- Adaptive frequency hopping (AFH) for reducing radio frequency interference.
A simplified block diagram of the module is depicted in the figure above.
- BT Core Specification Version 6.0, including the following support:
 - Low energy(LE) isochronous channels
 - LE power control
 - LE enhanced connection update
 - LE channel classification
 - LE audio
 - LE Long Range(LE-LR)

IEEE 802.15.4/Thread Key Feature

- Support IEEE 802.15.4/Thread that can act as Border Router.

2. General Specification

2.1 General Specification

Model Name	AP5281SR
Product Description	1T1R 802.11 a/b/g/n/ac/ax Wi-Fi 6E + BT 6.0+ IEEE 802.15.4/Thread Module
Dimension	L x W : 7.9 x 6.3 (typical) mm , H : 1.1 (Maximum) mm
WiFi Interface	Support SDIO V3.0/ 2.0
BT Interface	UART / PCM
Operating temperature	-30°C to 85°C
Storage temperature	-40°C to 125°C
Humidity	Operating Humidity 10% to 95% Non-Condensing

Note: The optimal RF performance specified in the data sheet, however, is guaranteed only -10 °C to +55 °C and 3.3V < VBAT < 3.8V without derating performance.

2.2 DC Characteristics

2.2.1 Absolute Maximum Ratings

Symbol	Description	Min.	Max.	Unit
VBAT	Input supply Voltage	3.0	5.0	V
VDDIO	Digital/Bluetooth/SDIO/ I/O Voltage	1.5	2.07	V

Note : RF performance is optimal for 3.3V ≤ VBAT ≤ 3.8V. For 2.5V ≤ VBAT < 3.2V, device radios will operate but RF performance will degrade.

2.2.2 Recommended Operating Rating

The module requires two power supplies: VBAT and VDDIO.

Voltage rails	Min.	Typ.	Max.	Unit
VBAT	3.3	3.6	3.8	V
VDDIO	1.62	1.8	1.98	V

VBAT current consumption 1000mA(Peak), when VBAT = 3.6V

The module requires two power supplies: other Digital I/O Pins.

For VDDIO=1.8V	Min.	Max.	Unit
Input high voltage	$0.65 \times \text{VDDIO}$	NA	V
Input low voltage	NA	$0.35 \times \text{VDDIO}$	V
Output high voltage @ 2mA	$\text{VDDIO} - 0.4$	NA	V
Output low voltage @ 2mA	NA	0.4	V

3. Wi-Fi RF Specification

3.1 2.4GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11 b/g/n/ac/ax & Wi-Fi compliant			
Frequency Range		2.400 GHz ~ 2.4835 GHz (2.4GHz ISM Band)			
Number of Channels		2.4GHz：Ch1 ~ Ch13			
Modulation		802.11b：DQPSK、DBPSK、CCK 802.11g/n：OFDM /64-QAM、16-QAM、QPSK、BPSK 802.11ac/ax：OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Resource Unit		Partial RU： BW20MHz：26T、52T、106T、242T			
Output Power , tolerance ± 1.5 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11b	1Mbps	2Mbps	5.5Mbps	11Mbps	
	18	18	18	18	
802.11g	6、9Mbps	12、18Mbps	24Mbps	36Mbps	48Mbps
	18	17.5	17.5	17	17
	54Mbps				
	17				
802.11n 20MHz	MCS0~2	MCS3	MCS4	MCS5	MCS6
	18	17.5	17.5	17	17
	MCS7				
	16				
802.11ac/ax 20MHz	MCS0~2/HE0~2	MCS3/HE3	MCS4/HE4	MCS5/HE5	MCS6/HE6
	18	17.5	17.5	17	17
	MCS7/HE7	MCS8/HE8	HE9	HE10	HE11
	16	15	14	14	14

Sensitivity, tolerance ± 2 dB				
CCK modulation PER $\leq 8\%$ 、OFDM modulation PER $\leq 10\%$				
802.11b	Data Rate	Spec.(dBm)		
	1Mbps	-96		
	2Mbps	-90		
	5.5Mbps	-88		
	11Mbps	-87		
802.11g	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-91	24Mbps	-83
	9Mbps	-88	36Mbps	-80
	12Mbps	-87	48Mbps	-76
	18Mbps	-85	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-77
	MCS1	-85	MCS5	-75
	MCS2	-84	MCS6	-72
	MCS3	-80	MCS7	-71
802.11ac/ax 20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0/HE0	-90	MCS6/HE6	-72
	MCS1/HE1	-85	MCS7/HE7	-71
	MCS2/HE2	-84	MCS8/HE8	-69
	MCS3/HE3	-80	HE9	-68
	MCS4/HE4	-77	HE10	-67
	MCS5/HE5	-75	HE11	-66
Maximum Input Level	802.11b : -10 dBm			
	802.11g/n/ax : -20 dBm			

3.2 5 GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11a/n/ac/ax & Wi-Fi compliant			
Frequency Range		5.15~5.35GHz 、 5.47~5.725GHz 、 5.725~5.85GHz （5GHz UNII Band）			
Number of Channels		5.15~5.35GHz ： Ch36 ~ Ch64 5.47~5.725GHz ： Ch100 ~ Ch144 5.725~5.85GHz ： Ch149 ~ Ch165			
Modulation		802.11a ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11n ： OFDM /64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ac ： OFDM /256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK 802.11ax ： OFDMA /1024-QAM 、 256-QAM 、 64-QAM 、 16-QAM 、 QPSK 、 BPSK			
Resource Unit		Partial RU ： BW20MHz ： 26T 、 52T 、 106T 、 242T BW40MHz ： 26T 、 52T 、 106T 、 242T 、 484T BW80MHz ： 26T 、 52T 、 106T 、 242T 、 484T 、 996T			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11a	Frequency (MHz)	6~9Mbps	12~18Mbps	24Mbps	36Mbps
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	48Mbps	54Mbps		
	5150~5350	15	15		
	5470~5725	15	15		
	5725~5845	15	15		
802.11n 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14		
	5470~5725	15	14		
	5725~5845	15	14		

802.11n 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7		
	5150~5350	15	14		
	5470~5725	15	14		
	5725~5845	15	14		
802.11ac 20MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	
	5150~5350	15	14	12	
	5470~5725	15	14	12	
	5725~5845	15	14	12	
802.11ac 40MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	14	12	12
	5470~5725	15	14	12	12
	5725~5845	15	14	12	12
802.11ac 80MHz	Frequency (MHz)	MCS0~2	MCS3	MCS4	MCS5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	MCS6	MCS7	MCS8	MCS9
	5150~5350	15	14	12	12
	5470~5725	15	14	12	12
	5725~5845	15	14	12	12
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15

	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	14	12	12
	5470~5725	15	14	12	12
	5725~5845	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5725	10	10		
	5725~5845	10	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	14	12	12
	5470~5725	15	14	12	12
	5725~5845	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5725	10	10		
	5725~5845	10	10		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5150~5350	15	15	15	15
	5470~5725	15	15	15	15
	5725~5845	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5150~5350	15	14	12	12
	5470~5725	15	14	12	12
	5725~5845	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5150~5350	10	10		
	5470~5725	10	10		
	5725~5845	10	10		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB, OFDM modulation PER $\leq 10\%$				
802.11a	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	6Mbps	-90	24Mbps	-83
	9Mbps	-90	36Mbps	-80
	12Mbps	-88	48Mbps	-75
	18Mbps	-86	54Mbps	-73
802.11n_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS4	-79
	MCS1	-88	MCS5	-76
	MCS2	-86	MCS6	-73
	MCS3	-83	MCS7	-72
802.11n_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS4	-77
	MCS1	-86	MCS5	-72
	MCS2	-83	MCS6	-70
	MCS3	-80	MCS7	-69
802.11ac_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-90	MCS5	-75
	MCS1	-88	MCS6	-73
	MCS2	-86	MCS7	-70
	MCS3	-83	MCS8	-68
	MCS4	-79		
802.11ac_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-88	MCS5	-72
	MCS1	-86	MCS6	-70
	MCS2	-83	MCS7	-69
	MCS3	-80	MCS8	-65
	MCS4	-76	MCS9	-64
802.11ac_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	MCS0	-85	MCS5	-68
	MCS1	-82	MCS6	-67
	MCS2	-79	MCS7	-65
	MCS3	-76	MCS8	-62
	MCS4	-73	MCS9	-61

802.11ax_20MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-90	HE6	-73
	HE1	-88	HE7	-70
	HE2	-86	HE8	-68
	HE3	-83	HE9	-64
	HE4	-79	HE10	-59
	HE5	-75	HE11	-57
802.11ax_40MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-70
	HE1	-86	HE7	-69
	HE2	-83	HE8	-65
	HE3	-80	HE9	-64
	HE4	-76	HE10	-60
	HE5	-72	HE11	-55
802.11ax_80MHz	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-85	HE6	-67
	HE1	-82	HE7	-65
	HE2	-79	HE8	-62
	HE3	-76	HE9	-61
	HE4	-73	HE10	-57
	HE5	-68	HE11	-53
Maximum Input Level	802.11a/n/ac/ax : -30 dBm			

3.3 6GHz RF Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25°C

Feature		Description			
WLAN Standard		IEEE 802.11ax Non-HT(802.11a) preamble for ack/beacon			
Frequency Range		5.955~7.115GHz			
Number of Channels		5955~6415MHz：6G1～6G93、6435~6515MHz：6G97～6G113 6535~6855MHz：6G117～6G181、6875~7115MHz：6G185～6G233			
Modulation		802.11ax：OFDMA /1024-QAM、256-QAM、64-QAM、16-QAM、QPSK、BPSK			
Resource Unit		Partial RU： BW20MHz：26T、52T、106T、242T BW40MHz：26T、52T、106T、242T、484T BW80MHz：26T、52T、106T、242T、484T、996T			
Output Power , tolerance ± 2 dB					
The transmit EVM quality & spectrum mask are compliant with IEEE 802.11 standard					
802.11ax 20MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15	15	15	15
	6435~6515	15	15	15	15
	6535~6875	15	15	15	15
	6895~7115	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	15	14	12	12
	6435~6515	15	14	12	12
	6535~6875	15	14	12	12
	6895~7115	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5955~6415	10	10		
	6435~6515	10	10		
	6535~6875	10	10		
	6895~7115	10	10		
802.11ax 40MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15	15	15	15
	6435~6515	15	15	15	15
	6535~6875	15	15	15	15
	6895~7115	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	15	14	12	12

	6435~6515	15	14	12	12
	6535~6875	15	14	12	12
	6895~7115	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5955~6415	10	10		
	6435~6515	10	10		
	6535~6875	10	10		
	6895~7115	10	10		
802.11ax 80MHz	Frequency (MHz)	HE0~2	HE3	HE4	HE5
	5955~6415	15	15	15	15
	6435~6515	15	15	15	15
	6535~6875	15	15	15	15
	6895~7115	15	15	15	15
	Frequency (MHz)	HE6	HE7	HE8	HE9
	5955~6415	15	14	12	12
	6435~6515	15	14	12	12
	6535~6875	15	14	12	12
	6895~7115	15	14	12	12
	Frequency (MHz)	HE10	HE11		
	5955~6415	10	10		
	6435~6515	10	10		
	6535~6875	10	10		
	6895~7115	10	10		

Note: The specifications of RF output power are subject to change to fulfill the safety regulation and requirements in end-user product.

Sensitivity, tolerance ± 2 dB, OFDM modulation PER $\leq 10\%$

802.11ax_20MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-88	HE6	-71
	HE1	-86	HE7	-68
	HE2	-84	HE8	-66
	HE3	-83	HE9	-62
	HE4	-77	HE10	-57
	HE5	-73	HE11	-55
802.11ax_40MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-86	HE6	-68
	HE1	-84	HE7	-67
	HE2	-81	HE8	-63

	HE3	-78	HE9	-62
	HE4	-74	HE10	-57
	HE5	-70	HE11	-53
802.11ax_80MHz SISO	Data Rate	Spec.(dBm)	Data Rate	Spec.(dBm)
	HE0	-83	HE6	-65
	HE1	-80	HE7	-63
	HE2	-77	HE8	-60
	HE3	-74	HE9	-59
	HE4	-71	HE10	-55
	HE5	-66	HE11	-51
Maximum Input Level	802.11ax : -30dBm			

4. Bluetooth Specification

4.1 Bluetooth Specification

Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25°C

Feature	Description
General Specification	
Bluetooth Standard	BDR 、 EDR(2Mbps & 3Mbps) 、 LE(1/2Mbps) 、 LELR(128/512Kbps)
Host Interface	UART
Frequency Band	2402 MHz ~ 2480 MHz
Number of Channels	79 channels for classic 、 40 channels for BLE
Modulation	GFSK, $\pi/4$ -DQPSK, 8DPSK
RF Specification	
Output Power , tolerance ± 1.5 dB	
	CL1 (dBm)
BDR Output Power	6
EDR Output Power	6
BLE Output Power	6
Sensitivity, tolerance ± 1.5 dB	
Sensitivity @ BER=0.1% for GFSK (1Mbps)	-88 dBm
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)	-90 dBm
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)	-84 dBm
Sensitivity @ PER=30.8% for LE (1Mbps)	-90 dBm
Sensitivity @ PER=30.8% for 2LE (2Mbps)	-90 dBm
Sensitivity @ PER=30.8% for LELR (125Kbps)	-102 dBm
Sensitivity @ PER=30.8% for LELR (500Kbps)	-96 dBm

Maximum Input Level	GFSK (1Mbps):-20dBm
	$\pi/4$ -DQPSK (2Mbps) :-20dBm
	8DPSK (3Mbps) :-20dBm

Note* : The Bluetooth BDR output power is able to be configured by firmware (hcd file).

5. 802.15.4 Specification

5.1 802.15.4 Specification

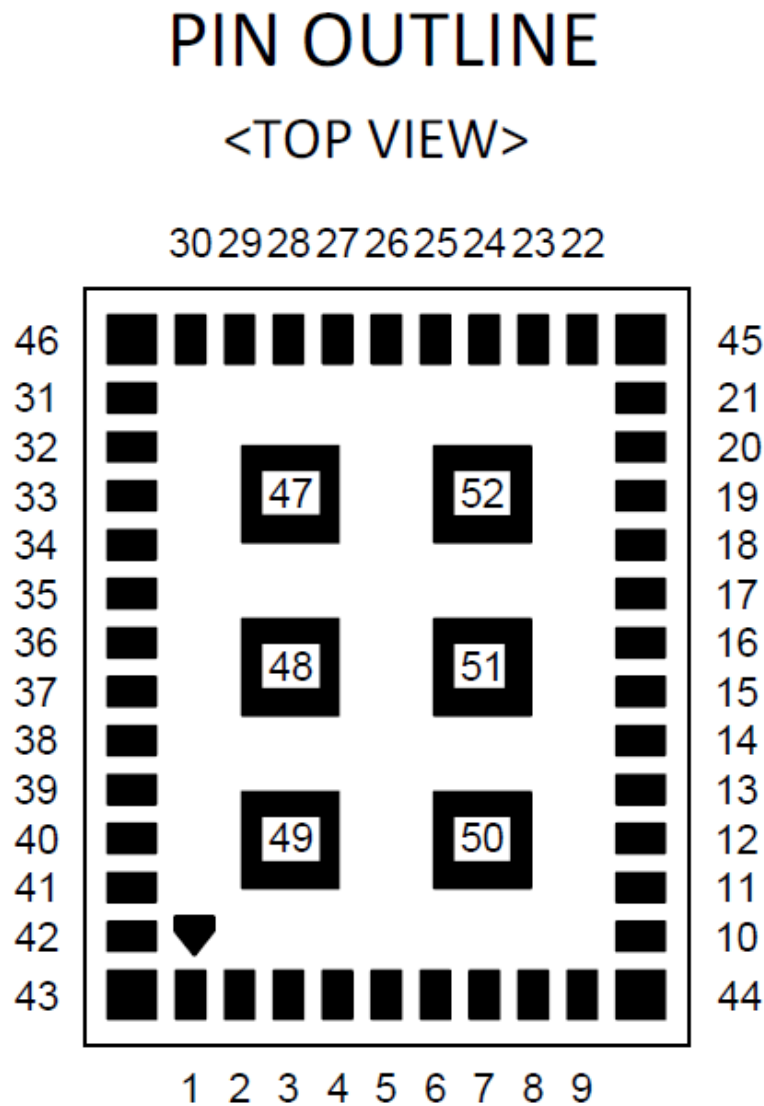
Conditions : VBAT=3.6V ; VDDIO=1.8V ; Temp:25°C

Feature	Description
General Specification	
Standard	IEEE 802.15.4
Host Interface	UART
Frequency Band	2405 MHz ~ 2480 MHz
Number of Channels	16 channels(channel 11~channel 26)
Channel list	2405(ch11) 、 2410(ch12)... 、 2480(ch26)
Modulation	OQPSK(250kbps)
RF Specification	
Output Power , tolerance ± 2 dB	
OQPSK Output Power*	8 dBm
Sensitivity, tolerance ± 2 dB	
Sensitivity @ PER=1% for 250kbps OQPSK	-97 dBm

Note* : The output power is able to be configured by firmware (hcd file).

6. Pin Definition

6.1 Pin Outline



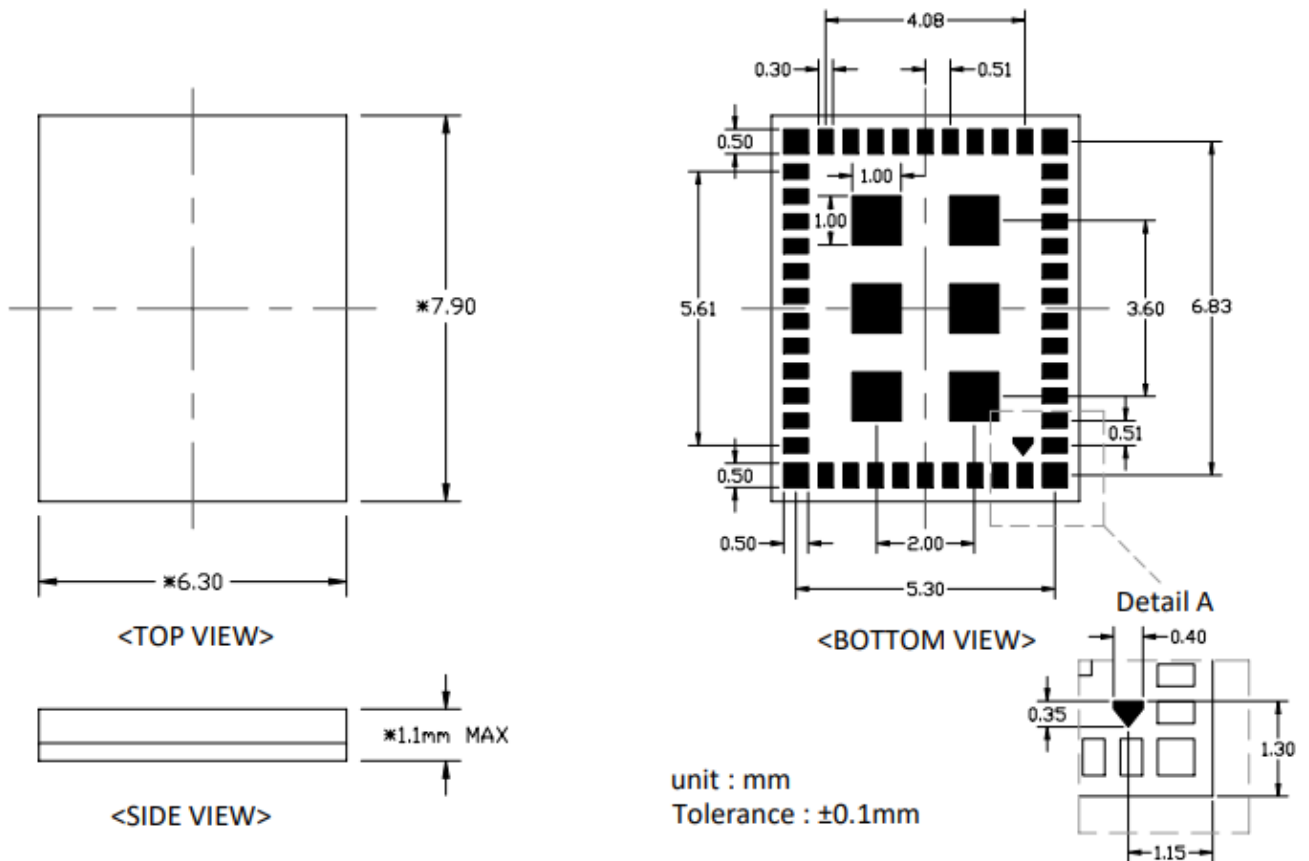
6.2 Pin Assignment

NO	Name	Type	Description
1	BT_DEV_WAKE	I	HOST wake-up Bluetooth device
2	BT_HOST_WAKE	O	Bluetooth device wake-up Host
3	WL_GPIO_5	I/O	WL_GPIO_5
4	WL_GPIO_4	I/O	WL_GPIO_4
5	GND	—	Ground connections
6	WL_GPIO_3	I/O	WL_GPIO_3
7	WL_GPIO_1	I/O	WL_GPIO_1
8	GND	—	Ground connections
9	GND	—	Ground connections
10	WL_BT_ANT	I/O	RF I/O port
11	GND	—	Ground connections
12	WL_GPIO_2	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
13	GPIO_0(WL_HOST_WAKE)	O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
14	WL_REG_ON	I	Power up/down internal regulators used by WiFi section
15	BT_REG_ON	I	Power up/down internal regulators used by BT section
16	VBAT	P	Main power voltage source input
17	VBAT	P	Main power voltage source input
18	GND	—	Ground connections
19	ABUCK_1V02	I	Internal Analog Buck voltage generation pin
20	ASR_VLX	O	Internal Analog Buck voltage generation pin
21	GND	—	Ground connections
22	CBUCK_0V72	I	Internal Analog Buck voltage generation pin
23	CSR_VLX	O	Internal Analog Buck voltage generation pin
24	GND	—	Ground connections
25	SDIO_DATA_CMD	I/O	SDIO command line
26	SDIO_DATA_0	I/O	SDIO data line 0
27	SDIO_DATA_CLK	I/O	SDIO clock line
28	SDIO_DATA_1	I/O	SDIO data line 1
29	SDIO_DATA_2	I/O	SDIO data line 2
30	SDIO_DATA_3	I/O	SDIO data line 3
31	LPO	I	External Low Power Clock input (32.768KHz)
32	GND	-	Ground connections

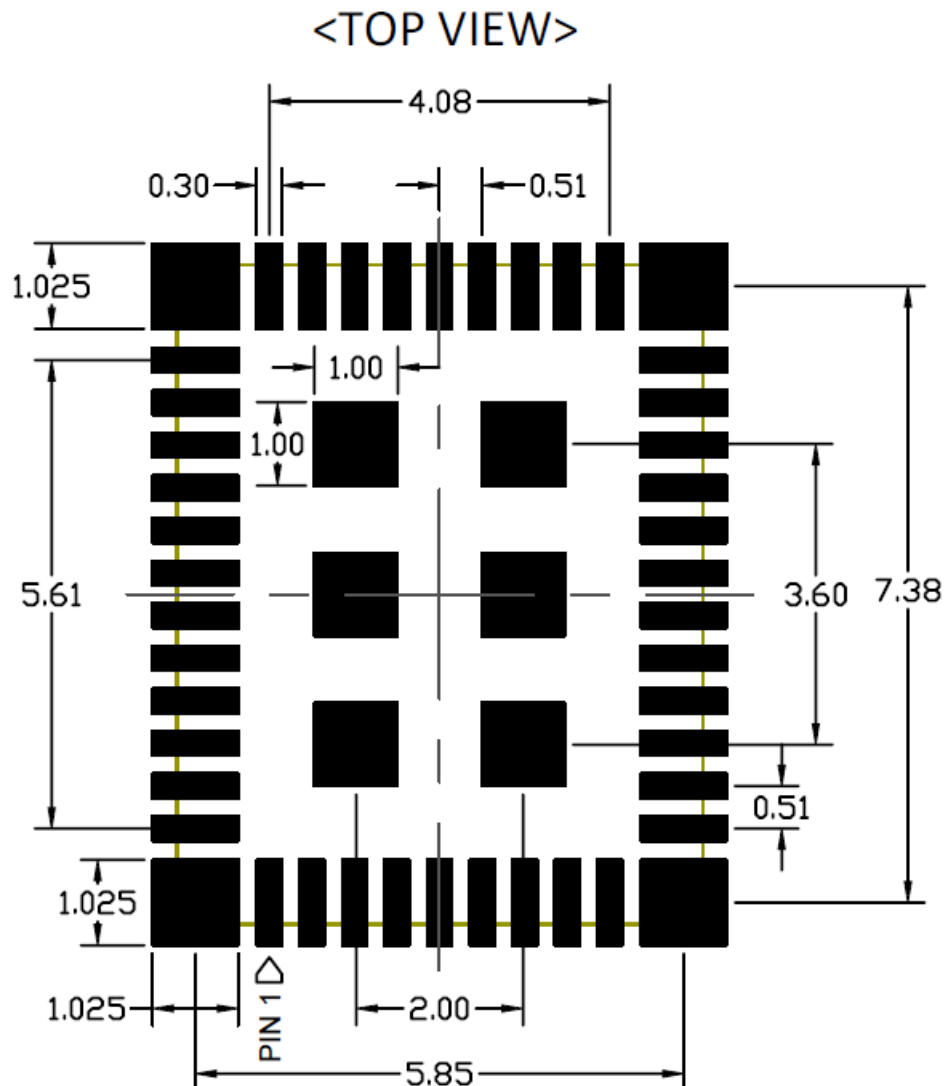
33	VDDIO_1V8	P	I/O Voltage supply input
34	BT_CLK_REQ	I/O	This pin can be programmed to be a GPIO, or the GCI external coexistence interface.
35	PCM_SYNC	I/O	PCM sync signal
36	PCM_CLK	I/O	PCM clock
37	PCM_IN	I	PCM data input
38	PCM_OUT	O	PCM Data output
39	UART_CTS_N	I	Bluetooth UART interface
40	UART_RTS_N	O	Bluetooth UART interface
41	UART_RXD	I	Bluetooth UART interface
42	UART_TXD	O	Bluetooth UART interface
43	GND	—	Ground connections
44	GND	—	Ground connections
45	GND	—	Ground connections
46	GND	—	Ground connections
47	GND	—	Ground connections
48	GND	—	Ground connections
49	GND	—	Ground connections
50	GND	—	Ground connections
51	GND	—	Ground connections
52	GND	—	Ground connections

7. Dimensions

7.1 Module Dimensions



7.2 Recommended footprint



- Solder paste layer design is generally the same as recommended footprint.
- If soldering quality with good wetting on upright side is essential for PQC, how to optimize the aperture design in the stencil to adjust the amount of solder paste would be crucial. In addition, a kind of stencil design with stepped thickness in partial area would be considered if the thickness of stencil is about 0.1mm or thinner. Please optimize the stencil design by manufacture engineer or contact AMPAK FAE for assistance.



8. External clock reference

External LPO signal characteristics

Parameter	Specification	Units
Nominal input frequency	32.768	kHz
Frequency accuracy	+/-25	ppm
Duty cycle	30 - 70	%
Input signal amplitude	1.8±0.09	V
Signal type	Square-wave or sine-wave	-
Input impedance	>100k	Ω
	<5	pF
Clock jitter (integrated over 300Hz – 15KHz)	<1	Hz
Output high voltage	0.7V _{io} - V _{io}	V

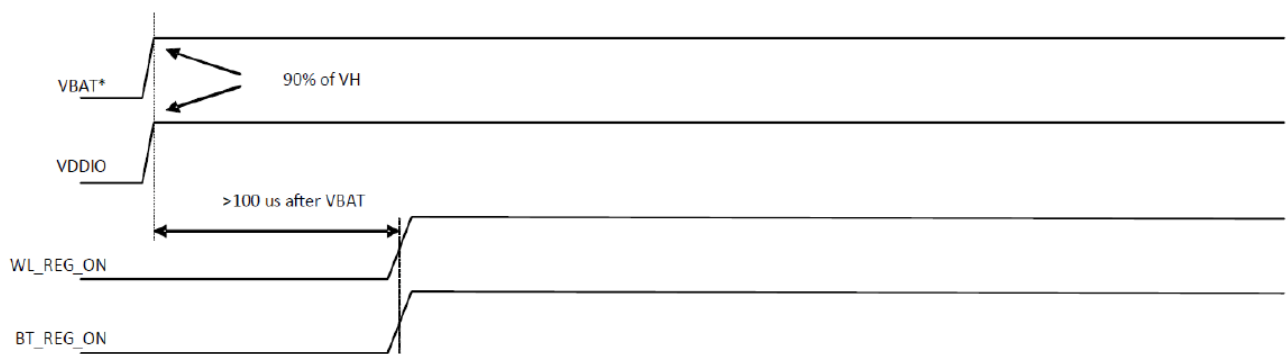
9. Host Interface Timing Diagram

9.1 Power-up Sequence Timing Diagram

The module has signals that allow the host to control power consumption by enabling or disabling the Bluetooth, WLAN and internal regulator blocks. These signals are described below.

Additionally, diagrams are provided to indicate proper sequencing of the signals for various operating states. The timing value indicated are minimum required values: longer delays are also acceptable.

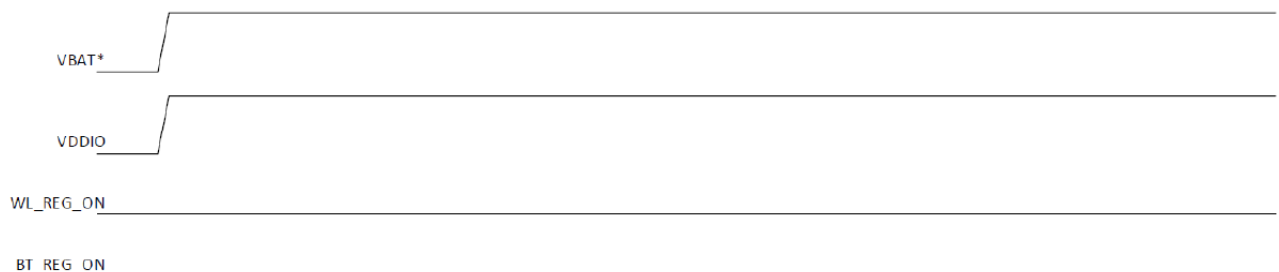
- **WL_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the WLAN section. When this pin is high, the regulators are enabled and the WLAN section is out of reset. When this pin is low the WLAN section is in reset.
- **BT_REG_ON**: Used by the PMU to power up or power down the internal regulators used by the BT section. Low asserting reset for Bluetooth. This pin has no effect on WLAN and does not control any PMU functions. This pin must be driven high or low (not left floating).



***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

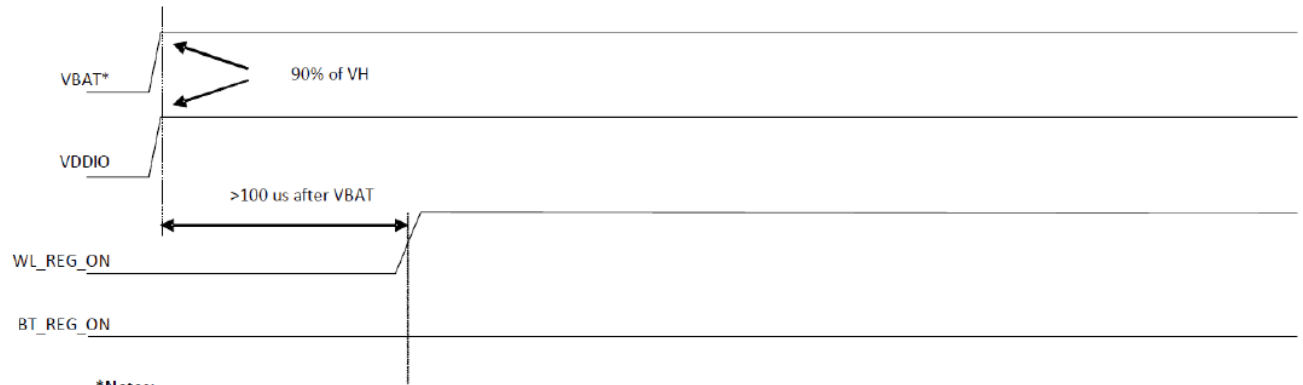
WLAN=ON, Bluetooth=ON



***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

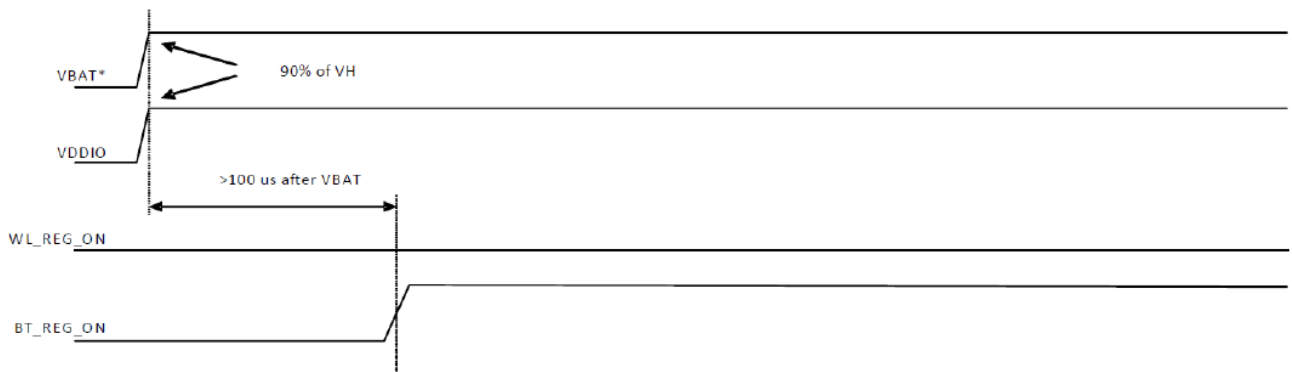
WLAN=OFF, Bluetooth=OFF



***Notes:**

1. The VBAT and VDDIO 10%–90% rise-time slopes must be greater than 50 microseconds/V.
2. VBAT should be up before or at the same time as VDDIO. VDDIO should NOT be present first or be held high before VBAT is high.

WLAN=ON, Bluetooth=OFF



WLAN=OFF, Bluetooth=ON

9.2 SDIO Interface Description

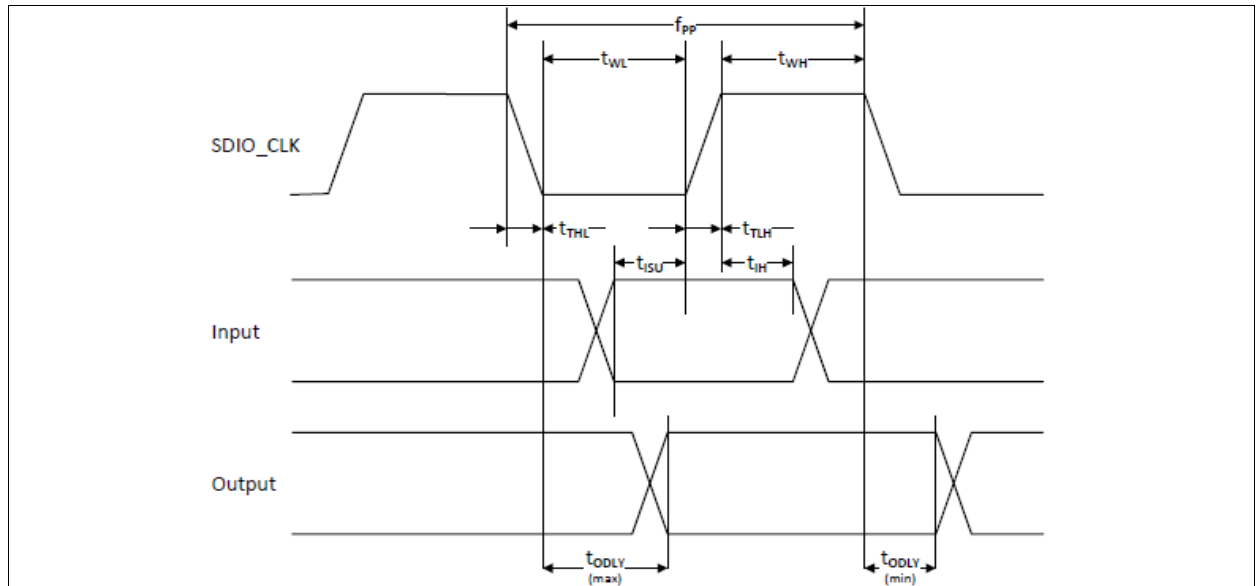
The module supports SDIO version 3.0 for all 1.8V 4-bit UHSI speeds: SDR50(100 MHz),SDR104(208MHz) and DDR50(50MHz, dual rates). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

- Function 0 Standard SDIO function (Max BlockSize / ByteCount = 32B)
- Function 1 Backplane Function to access the internal System On Chip (SOC) address space (Max BlockSize / ByteCount = 64B)
- Function 2 WLAN Function for efficient WLAN packet transfer through DMA (Max BlockSize/ByteCount=512B)

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

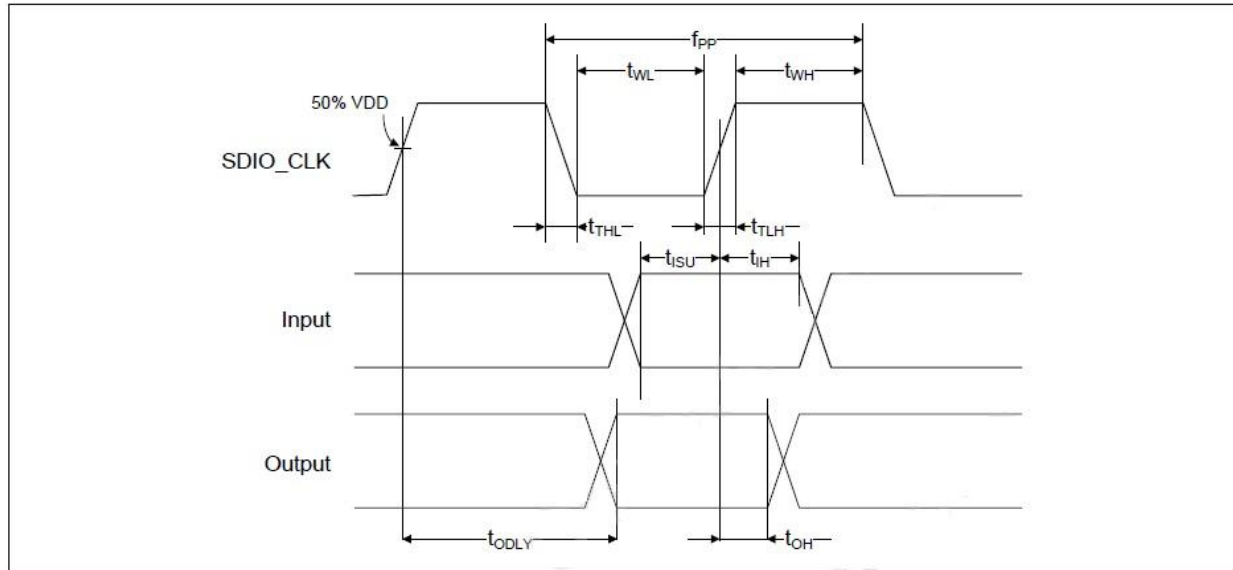
SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (All values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer mode	f_{PP}	0	–	25	MHz
Frequency – Identification mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	10	–	–	ns
Clock high time	t_{WH}	10	–	–	ns
Clock rise time	t_{TLH}	–	–	10	ns
Clock low time	t_{THL}	–	–	10	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup time	t_{ISU}	5	–	–	ns
Input hold time	t_{IH}	5	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer mode	t_{ODLY}	0	–	14	ns
Output delay time – Identification mode	t_{ODLY}	0	–	50	ns

- a. Timing is based on $CL \leq 40pF$ load on CMD and Data.
b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

SDIO High Speed Mode Timing Diagram



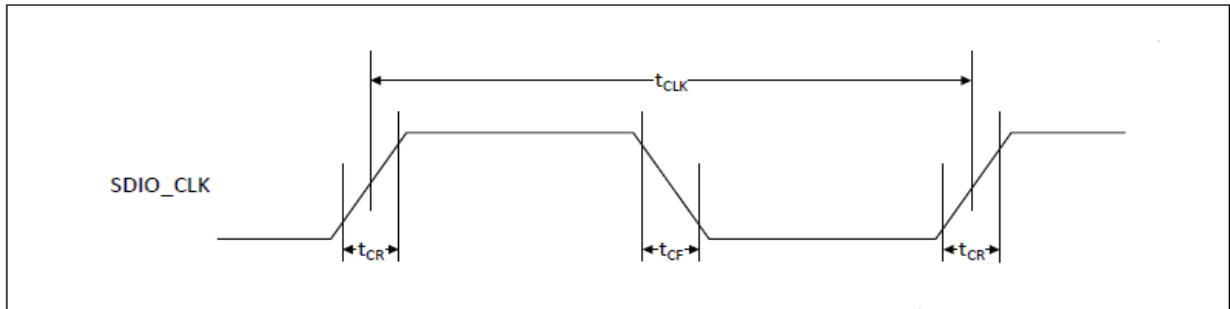
Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK (all values are referred to minimum V_{IH} and maximum V_{IL}^b)					
Frequency – Data Transfer Mode	f_{pp}	0	–	50	MHz
Frequency – Identification Mode	f_{OD}	0	–	400	kHz
Clock low time	t_{WL}	7	–	–	ns
Clock high time	t_{WH}	7	–	–	ns
Clock rise time	t_{TLH}	–	–	3	ns
Clock low time	t_{THL}	–	–	3	ns
Inputs: CMD, DAT (referenced to CLK)					
Input setup Time	t_{ISU}	6	–	–	ns
Input hold Time	t_{IH}	2	–	–	ns
Outputs: CMD, DAT (referenced to CLK)					
Output delay time – Data Transfer Mode	t_{ODLY}	–	–	14	ns
Output hold time	t_{OH}	2.5	–	–	ns
Total system capacitance (each line)	CL	–	–	40	pF

a. Timing is based on $CL \leq 40$ pF load on CMD and Data.

b. $\min(V_{IH}) = 0.7 \times V_{DDIO}$ and $\max(V_{IL}) = 0.2 \times V_{DDIO}$.

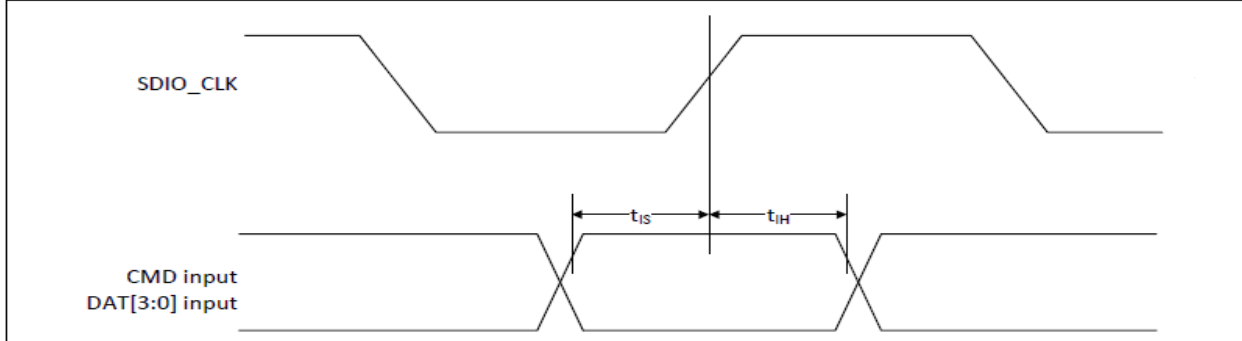
SDIO Bus Timing Specifications in SDR Modes

Clock timing (SDR Modes)



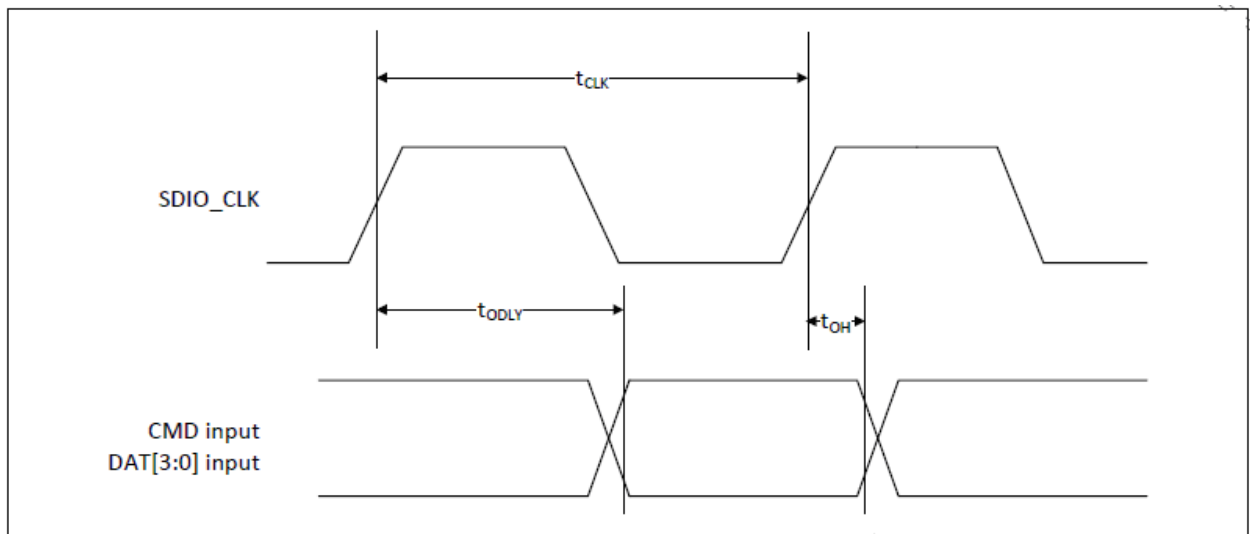
Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	40	—	ns	SDR12 mode
		20	—	ns	SDR25 mode
		10	—	ns	SDR50 mode
		4.8	—	ns	SDR104 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max) @100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max) @208 MHz, $C_{CARD} = 10$ pF
Clock duty	—	30	70	%	—

SDIO Bus Input timing (SDR Modes)



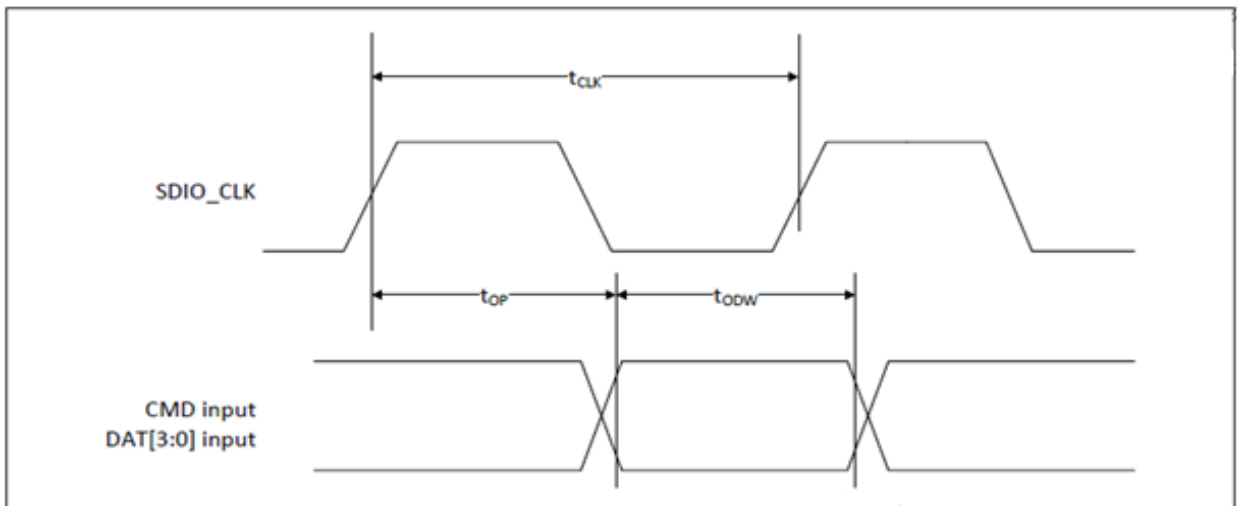
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.4	—	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	—	ns	$C_{CARD} = 5$ pF, VCT = 0.975V
SDR50 Mode				
t_{IS}	3.00	—	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	—	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

SDIO Bus output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	–	7.5	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	–	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	–	ns	Hold time at the t_{ODLY} (min) $C_L = 15$ pF

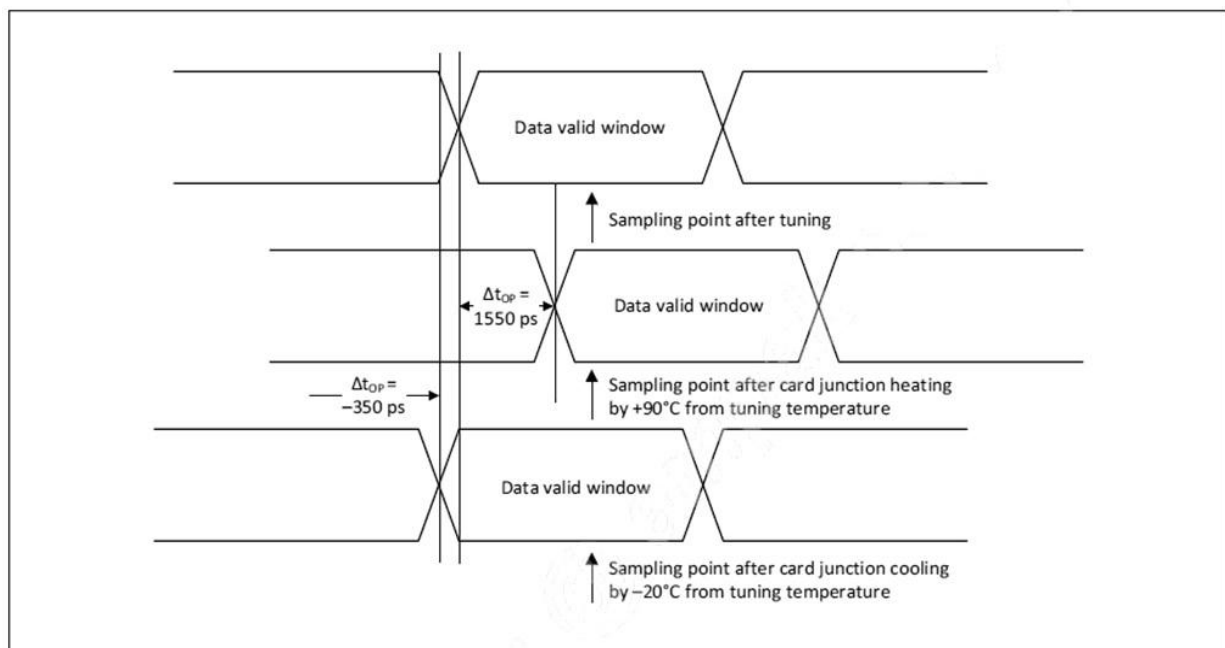
Card output timing (SDR Modes 100MHz to 208MHz)



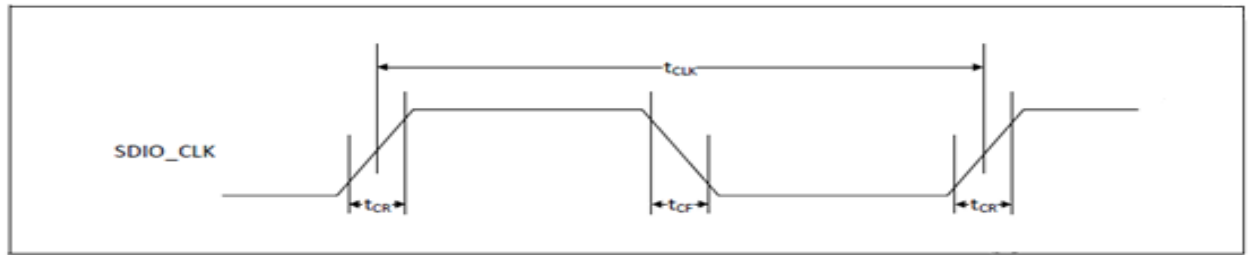
Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.60	—	UI	$t_{ODW}=2.88$ ns @ 208 MHz

- $\Delta t_{OP} = +1550$ ps for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350$ ps for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600$ ps for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

Δt_{OP} Consideration for Variable Data Window (SDR 104 Mode)

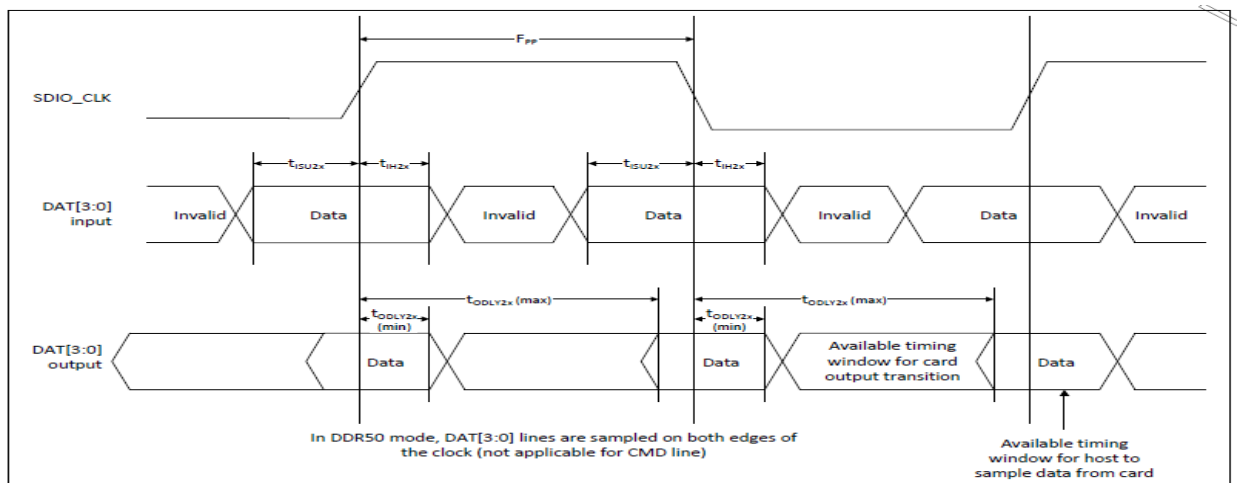


SDIO Bus Timing Specifications in DDR50 Mode



Parameter	Symbol	Minimum	Maximum	Unit	Comments
—	t_{CLK}	20	—	ns	DDR50 mode
—	t_{CR}, t_{CF}	—	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00$ ns (max) @50 MHz, $C_{CARD} = 10$ pF
Clock duty	—	45	55	%	—

Data Timing



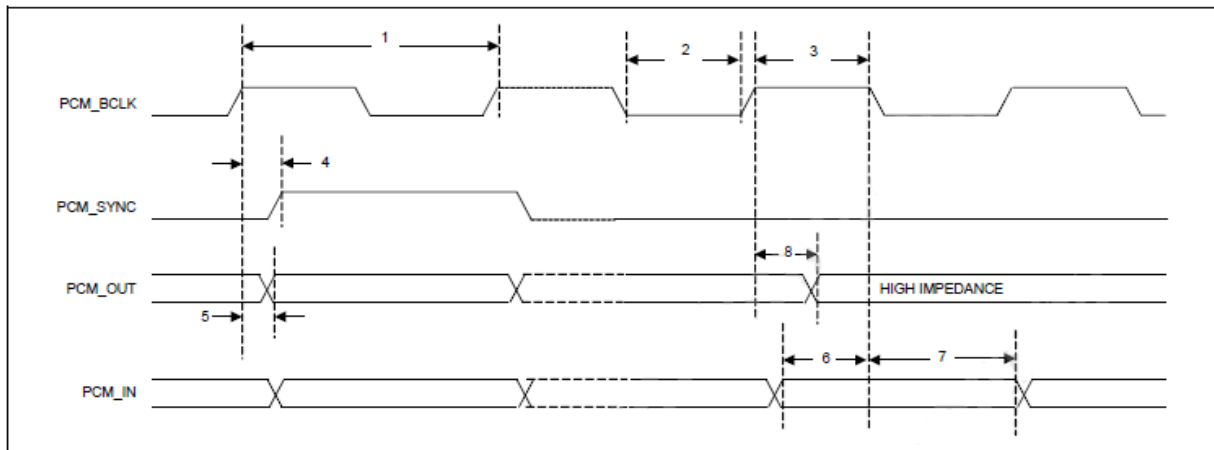
Parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t_{ISU}	6	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output CMD					
Output delay time	t_{ODLY}	—	13.7	ns	$C_{CARD} < 30$ pF (1 Card)
Output hold time	t_{OH}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)
Input DAT					
Input setup time	t_{ISU2x}	3	—	ns	$C_{CARD} < 10$ pF (1 Card)
Input hold time	t_{IH2x}	0.8	—	ns	$C_{CARD} < 10$ pF (1 Card)
Output DAT					
Output delay time	t_{ODLY2x}	—	7.5	ns	$C_{CARD} < 25$ pF (1 Card)
Output hold time	t_{ODLY2x}	1.5	—	ns	$C_{CARD} < 15$ pF (1 Card)

9.3 PCM Interface Description

The PCM Interface on the AP5281SR can connect to linear PCM Codec devices in master or slave mode. In master mode, the AP5281SR generates the PCM_CLK and PCM_SYNC signals, and in slave mode, these signals are provided by another master on the PCM interface and are inputs to the AP5281SR. The configuration of the PCM interface may be adjusted by the host through the use of vendor-specific HCI commands.

Short Frame Sync, Master Modem

PCM Timing Diagram (Short Frame Sync, Master Mode)

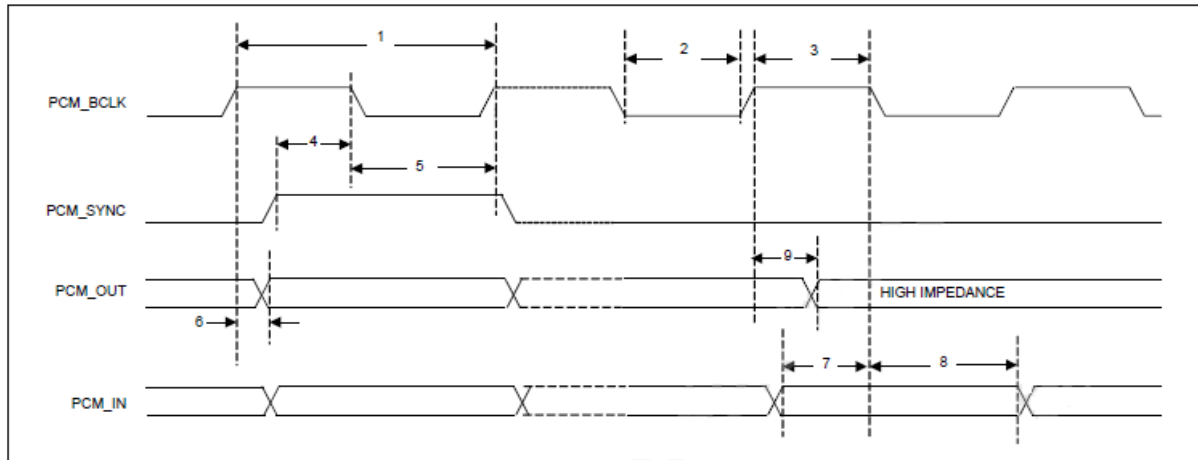


PCM Interface Timing Specifications (Short Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency		–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Slave Mode

PCM Timing Diagram (Short Frame Sync, Slave Mode)

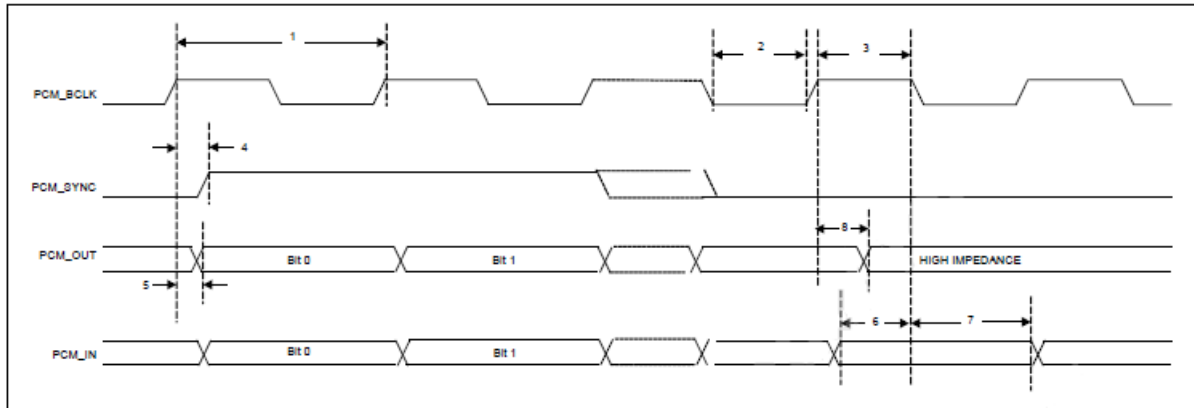


PCM Interface Timing Specifications (Short Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Master Mode

PCM Timing Diagram (Long Frame Sync, Master Mode)

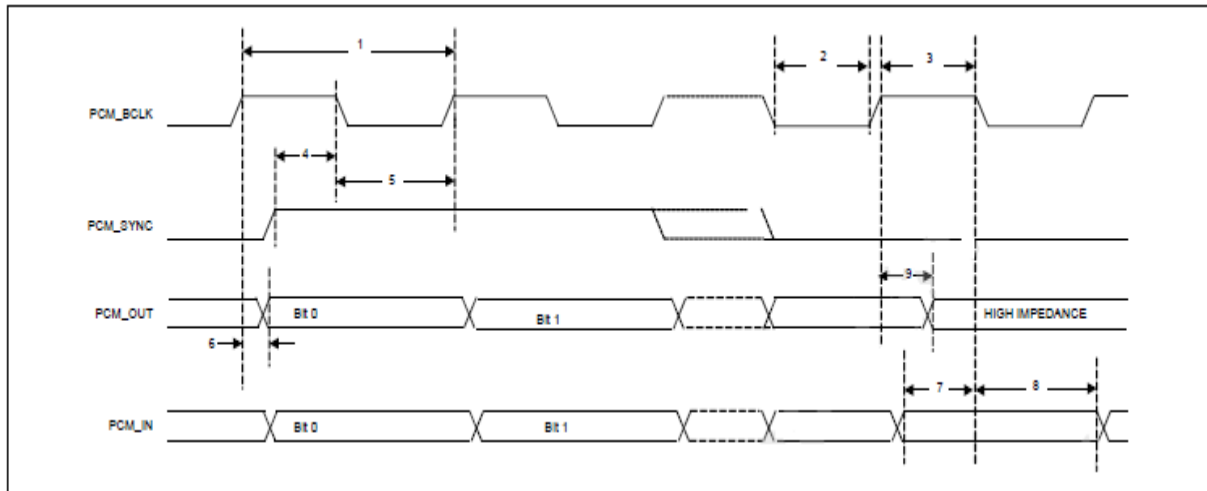


PCM Interface Timing Specifications (Long Frame Sync, Master Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC delay	0	–	25	ns
5	PCM_OUT delay	0	–	25	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns
8	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Long Frame Sync, Slave Mode

PCM Timing Diagram (Long Frame Sync, Slave Mode)

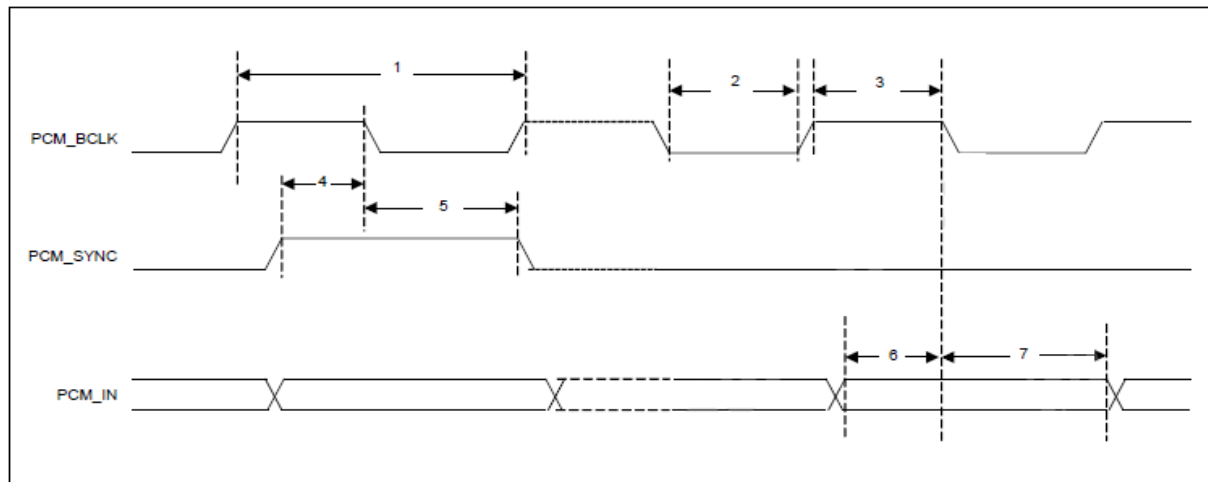


PCM Interface Timing Specifications (Long Frame Sync, Slave Mode)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	12	MHz
2	PCM bit clock low	41	–	–	ns
3	PCM bit clock high	41	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_OUT delay	0	–	25	ns
7	PCM_IN setup	8	–	–	ns
8	PCM_IN hold	8	–	–	ns
9	Delay from rising edge of PCM_BCLK during last bit period to PCM_OUT becoming high impedance	0	–	25	ns

Short Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Short Frame Sync)

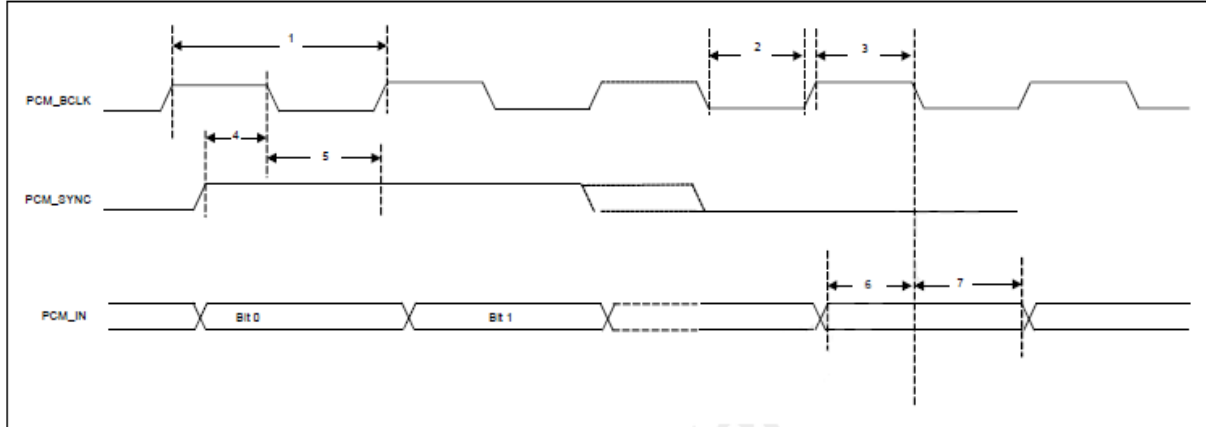


PCM Burst Mode (Receive Only, Short Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

Long Frame Sync, Burst Mode

PCM Burst Mode Timing (Receive Only, Long Frame Sync)



PCM Burst Mode (Receive Only, Long Frame Sync)

Reference	Characteristics	Minimum	Typical	Maximum	Unit
1	PCM bit clock frequency	–	–	24	MHz
2	PCM bit clock low	20.8	–	–	ns
3	PCM bit clock high	20.8	–	–	ns
4	PCM_SYNC setup	8	–	–	ns
5	PCM_SYNC hold	8	–	–	ns
6	PCM_IN setup	8	–	–	ns
7	PCM_IN hold	8	–	–	ns

9.4 UART Interface Description

The UART is a standard 4-wire interface (RX, TX, RTS, and CTS) with adjustable baud rates from 9600 bps to 4.0 Mbps. The interface features an automatic baud rate detection capability that returns a baud rate selection. Alternatively, the baud rate may be selected through a vendor-specific UART HCI command.

UART has a 1040-byte receive FIFO and a 1040-byte transmit FIFO to support EDR. Access to the FIFOs is conducted through the AHB interface through either DMA or the CPU. The UART supports the Bluetooth 5.0 UART HCI specification: H4, a custom Extended H4, and H5. The default baud rate is 115.2 Kbaud.

The UART supports the 3-wire H5 UART transport, as described in the Bluetooth specification (Three-wire UART Transport Layer). Compared to H4, the H5 UART transport reduces the number of signal lines required by eliminating the CTS and RTS signals.

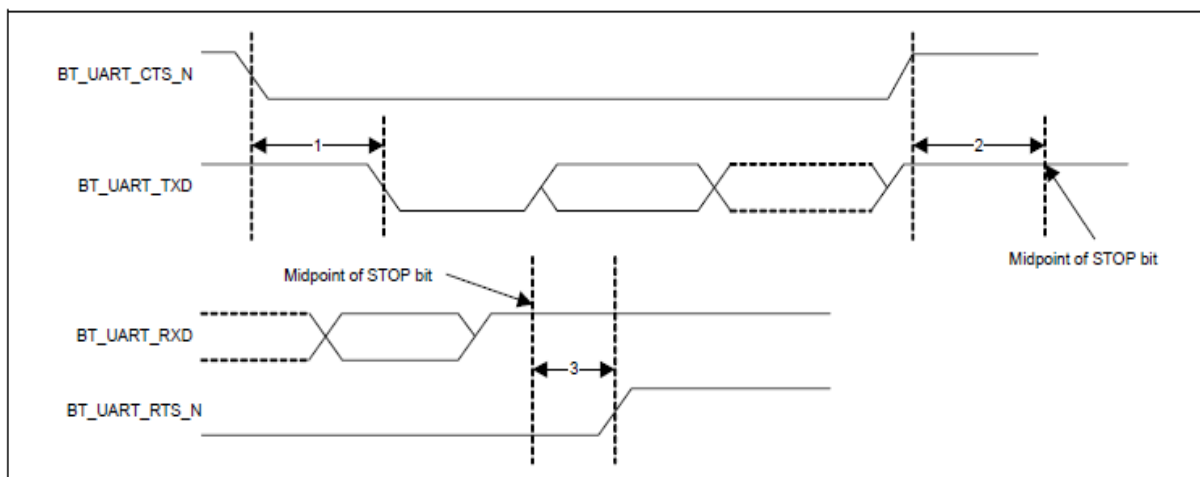
The UART can perform XON/XOFF flow control and includes hardware support for the Serial Line Input Protocol (SLIP). It can also perform wake-on activity. For example, activity on the RX or CTS inputs can wake the chip from a sleep state.

Normally, the UART baud rate is set by a configuration record downloaded after device reset, or by automatic baud rate detection, and the host does not need to adjust the baud rate. Support for changing the baud rate during normal HCI UART operation is included through a vendor-specific command that allows the host to adjust the contents of the baud rate registers. The UARTs operate correctly with the host UART as long as the combined baud rate error of the two devices is within $\pm 2\%$.

Example of Common Baud Rates

<i>Desired Rate</i>	<i>Actual Rate</i>	<i>Error (%)</i>
4000000	4000000	0.00
3692000	3692308	0.01
3000000	3000000	0.00
2000000	2000000	0.00
1500000	1500000	0.00
1444444	1454544	0.70
921600	923077	0.16
460800	461538	0.16
230400	230796	0.17
115200	115385	0.16
57600	57692	0.16
38400	38400	0.00
28800	28846	0.16
19200	19200	0.00
14400	14423	0.16
9600	9600	0.00

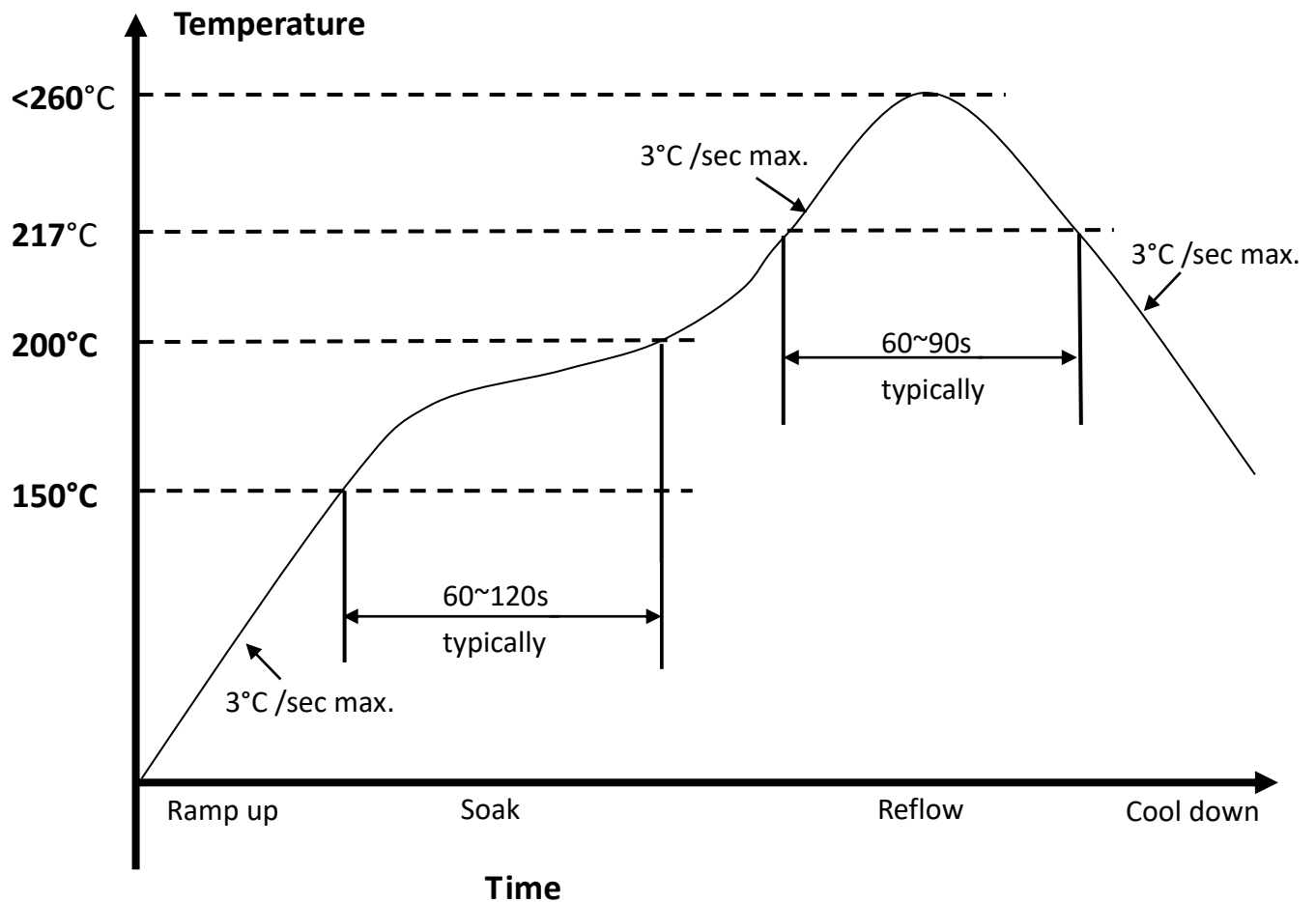
UART Timing



UART Timing Specifications

<i>Ref</i>	<i>Characteristics</i>	<i>Min.</i>	<i>Typ.</i>	<i>Max.</i>	<i>Unit</i>
1	Delay time, BT_UART_CTS_N low to BT_UART_TXD valid	–	–	1.5	Bit periods
2	Setup time, BT_UART_CTS_N high before midpoint of stop bit	–	–	0.5	Bit periods
3	Delay time, midpoint of stop bit to BT_UART_RTS_N high	–	–	0.5	Bit periods

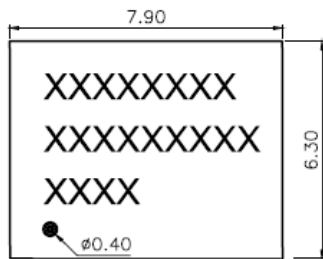
10. Recommended Reflow Profile



1. Referred to IPC/JEDEC standard
2. Peak Temperature : <260°C (Time within 5°C of actual Peak Temperature 20-40 seconds)
3. Cycle of Reflow : 2 times max.
4. Adding Nitrogen (N₂) to implement 2000ppm or less of oxygen concentration during reflow process is recommended.
5. If the shelf time is exceeded, be sure baking step to remove the moisture from the component

11. Package Information

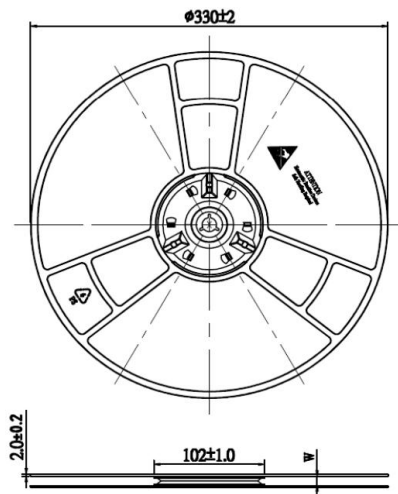
11.1 Marking



Rows	Content	Note
Row 1	XXXXXXXXXX	Model Name
Row 2	XXXXXXXXXX or JXXXXXXXXXX (8 digitals or 9 digitals)	Lot Code
Row 3	YYWW	Date Code
Row 4	Pin 1 a circular point	Pin 1 indicator

11.2 Tape & Reel Data

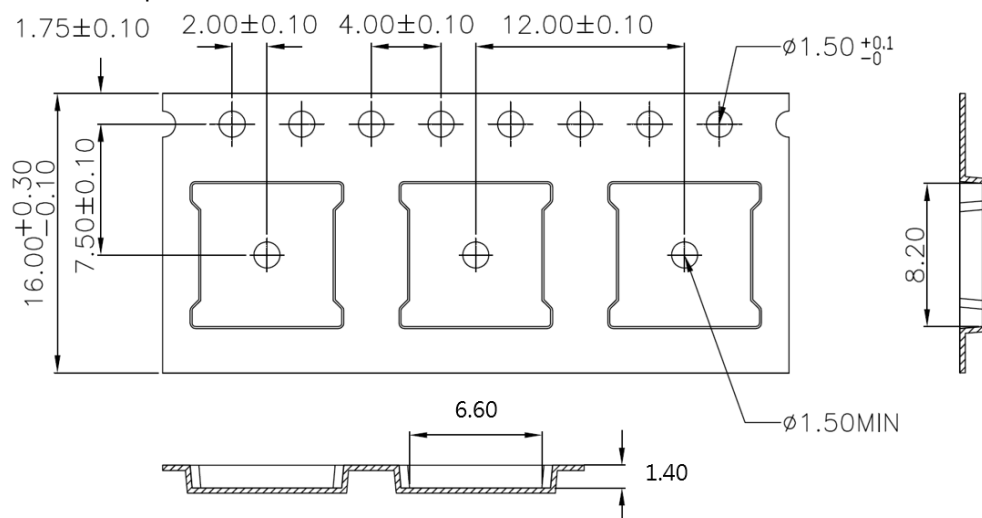
Reel



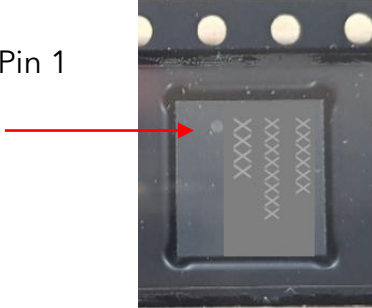
(unit :mm)

Carrier tape

(unit :mm)

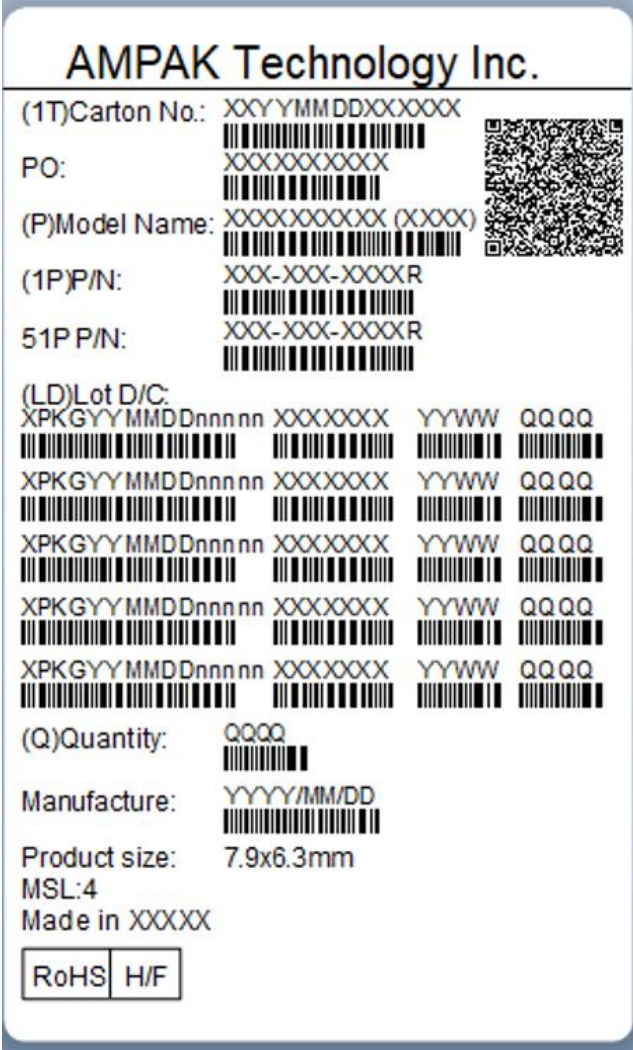


11.3 Tape & Reel Packing

Items	Photo	Description
1	 Pin 1	Pin 1 indicator in carrier tape
2		13" W16.0mm Reel
3		Humidity Indicator Card & Desiccant inside
4		MSL Caution label on top side of Al bag
5		Anti-static and humidity notice on top side of Al bag

Inner box (Box) label
(Reel label/Al Bag label/Box label)

The label content includes barcode
and QR CODE

9		5 inner boxes per outer box (Carton) Quantity: 10000pcs/outer box (Carton)
10		Outer box (Carton) Quantity: 10000pcs/outer box (Carton)
11	 AMPAK Technology Inc. (1T)Carton No.: XXXYMMDDXXX PO: XXXXXXXXXX (P)Model Name: XXXXXXXXX (XXXX) (1P)P/N: XXX-XXX-XXXXR 51P P/N: XXX-XXX-XXXXR (LD)Lot D/C: XPKGYMMDDnnnnn XXXXXXXX YYWW QQQQ XPKGYMMDDnnnnn XXXXXXXX YYWW QQQQ XPKGYMMDDnnnnn XXXXXXXX YYWW QQQQ XPKGYMMDDnnnnn XXXXXXXX YYWW QQQQ XPKGYMMDDnnnnn XXXXXXXX YYWW QQQQ (Q)Quantity: QQQQ Manufacture: YYYY/MM/DD Product size: 7.9x6.3mm MSL:4 Made in XXXXX RoHS H/F	Outer box (Carton) label The label content includes barcode and QR CODE